**In the Claims**:

Claims 1-14 (Cancelled).

15. (Currently Amended) A computer system comprising:

at least one peripheral for generating interrupt requests;

an interrupt pending register for storing the interrupt requests;

a microprocessor for processing interrupts;

an interrupt control circuit coupled to said interrupt pending register and said microprocessor for providing an interrupt command to said microprocessor based upon the stored interrupt requests; and

an auxiliary interrupt control circuit coupled to said at least one peripheral and said microprocessor for generating a bit string identifying an active bit stored in the interrupt pending register corresponding to a highest priority interrupt request to be processed and providing the bit string to said microprocessor;

said microprocessor identifying and processing an interrupt corresponding to the highest priority interrupt request based upon the bit string and the interrupt command without having to read said interrupt pending register.

16. (Previously Presented) The computer system of Claim 15 wherein said auxiliary interrupt control circuit comprises an encoder for generating the bit string based upon a position of the active bit in the interrupt pending register.

17. (Currently Amended) The computer system of Claim 16 further comprising an auxiliary register coupled to said ~~priority~~ interrupt pending register for storing a copy of the interrupt requests, and wherein said encoder generates the bit string based upon the interrupt requests stored in said auxiliary register.

18. (Previously Presented) The computer system of Claim 16 wherein said auxiliary interrupt control circuit further comprises at least one interrupt priority mask circuit coupled to said encoder, and wherein said encoder generates the bit string responsive to said at least one interrupt priority mask circuit.

19. (Previously Presented) The computer system of Claim 18 wherein said auxiliary interrupt control circuit further comprises a memory coupled to said at least one priority mask circuit for storing interrupt priority values for configuring said at least one priority mask circuit.

20. (Previously Presented) The computer system of Claim 15 wherein the bit string comprises a first bit string; and wherein said auxiliary interrupt control circuit further generates and provides to said microprocessor a second bit string identifying a position of a last active bit in said interrupt pending register.

21. (Previously Presented) The computer system of Claim 20 wherein said auxiliary interrupt control circuit

further generates and provides to said microprocessor a third bit string identifying a total number of active bits in said interrupt pending register.

22. (Previously Presented) The computer system of Claim 15 wherein the identified active bit of the highest priority interrupt request is the first active bit in the pending interrupt register.

23. (Currently Amended) An auxiliary interrupt control circuit for use in a computer system comprising at least one peripheral for generating interrupt requests, an interrupt pending register for storing the interrupt requests, a microprocessor for processing interrupts, and an interrupt control circuit associated with said microprocessor, said auxiliary control circuit comprising:

an auxiliary register coupled to said priority interrupt register for storing a copy of the interrupt requests; and

an encoder coupled to said auxiliary register and the microprocessor for generating a bit string identifying an active bit stored in the auxiliary register corresponding to a highest priority interrupt request to be processed and providing the bit string to the microprocessor so that the microprocessor identifies and processes an interrupt corresponding to the highest priority interrupt request based upon the bit string and an interrupt command without having to read the interrupt pending register.

24. (Previously Presented) The auxiliary interrupt

control circuit of Claim 23 wherein said encoder generates the bit string based upon a position of the active bit in the interrupt pending register.

25. (Previously Presented) The auxiliary interrupt control circuit of Claim 23 further comprising at least one interrupt priority mask circuit coupled to said encoder, and wherein said encoder generates the bit string responsive to said at least one interrupt priority mask circuit.

26. (Previously Presented) The auxiliary interrupt control circuit of Claim 25 further comprising a memory coupled to said at least one priority mask circuit for storing interrupt priority values for configuring said at least one priority mask circuit.

27. (Previously Presented) The auxiliary interrupt control circuit of Claim 23 wherein the bit string comprises a first bit string; and wherein said encoder further generates and provides to the microprocessor a second bit string identifying a position of a last active bit in said auxiliary register.

28. (Previously Presented) The auxiliary interrupt control circuit of Claim 27 wherein said encoder further generates and provides to the microprocessor a third bit string identifying a total number of active bits in said auxiliary register.

29. (Currently Amended) A peripheral to be coupled

to a microprocessor having an associated interrupt control circuit, the peripheral comprising:

a peripheral controller for generating interrupt requests;

an interrupt pending register for storing the interrupt requests; and

an auxiliary interrupt control circuit coupled to said interrupt pending register and the microprocessor for generating a bit string identifying an active bit stored in said interrupt pending register corresponding to a highest priority interrupt request to be processed and providing the bit string to the microprocessor so that the microprocessor identifies and processes an interrupt corresponding to the highest priority interrupt request based upon the bit string and an interrupt command without having to read said interrupt pending register

30. (Previously Presented) The peripheral of Claim 29 wherein said auxiliary interrupt control circuit comprises an encoder for generating the bit string based upon a position of the active bit in the interrupt pending register.

31. (Previously Presented) The peripheral of Claim 30 wherein said auxiliary interrupt control circuit further comprises at least one interrupt priority mask circuit coupled to said encoder, and wherein said encoder generates the bit string responsive to said at least one interrupt priority mask circuit.

32. (Previously Presented) The peripheral of Claim

29 wherein the bit string comprises a first bit string; and wherein said auxiliary interrupt control circuit further generates and provides to said microprocessor a second bit string identifying a position of a last active bit in said interrupt pending register.

33. (Previously Presented) The peripheral of Claim 32 wherein said auxiliary interrupt control circuit further generates and provides to said microprocessor a third bit string identifying a total number of active bits in said interrupt pending register.

34. (Currently Amended) A method for processing peripheral interrupts comprising:

generating interrupt requests using at least one peripheral and storing the interrupt requests in a pending interrupt register;

generating a bit string identifying an active bit corresponding to a highest priority interrupt request in the pending interrupt register to be processed; and

identifying and processing an interrupt corresponding to the highest priority interrupt request based upon the bit string without having to read the interrupt pending register.

35. (Previously Presented) The method of Claim 34 wherein the identified active bit of the highest priority interrupt request is the first active bit in the pending interrupt register.

36. (Previously Presented) The method of Claim 34 wherein the bit string comprises a first bit string, and further comprising generating a second bit string identifying a last active bit in the interrupt pending register prior to identifying and processing.

37. (Previously Presented) The method of Claim 36 further comprising generating a third bit string identifying a total number of active bits in the interrupt pending register prior to identifying and processing.

38. (Previously Presented) The method of Claim 34 wherein generating the bit string comprises copying the interrupt requests from the interrupt pending register to an auxiliary register and generating the bit string based upon the copied interrupt requests.